# PK0205_PGL12G_LPG144

(version number: Version 1.0)

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**Shenzhen Ziguang Tongchuang Electronics Co., Ltd.**

# Document version revision record

| VERSION NUMBER | RELEASE DATE | REVISION HISTORY |
|---|---|---|
| V1.0 | 2019/03/23 | initial issue |
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## Glossary

PODs : Package Outline Drawing

QFP : Quad Flat Package

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# 1. PACKAGING INTRODUCTION

The PGL12G_LPG144 product is available in a Wire bonded square flat QFP package. The package size is 22 mm x 22 mm (including pin length). The number of pins is 144 and the pin spacing is 0.5 mm, the maximum package thickness is 1.60 mm.

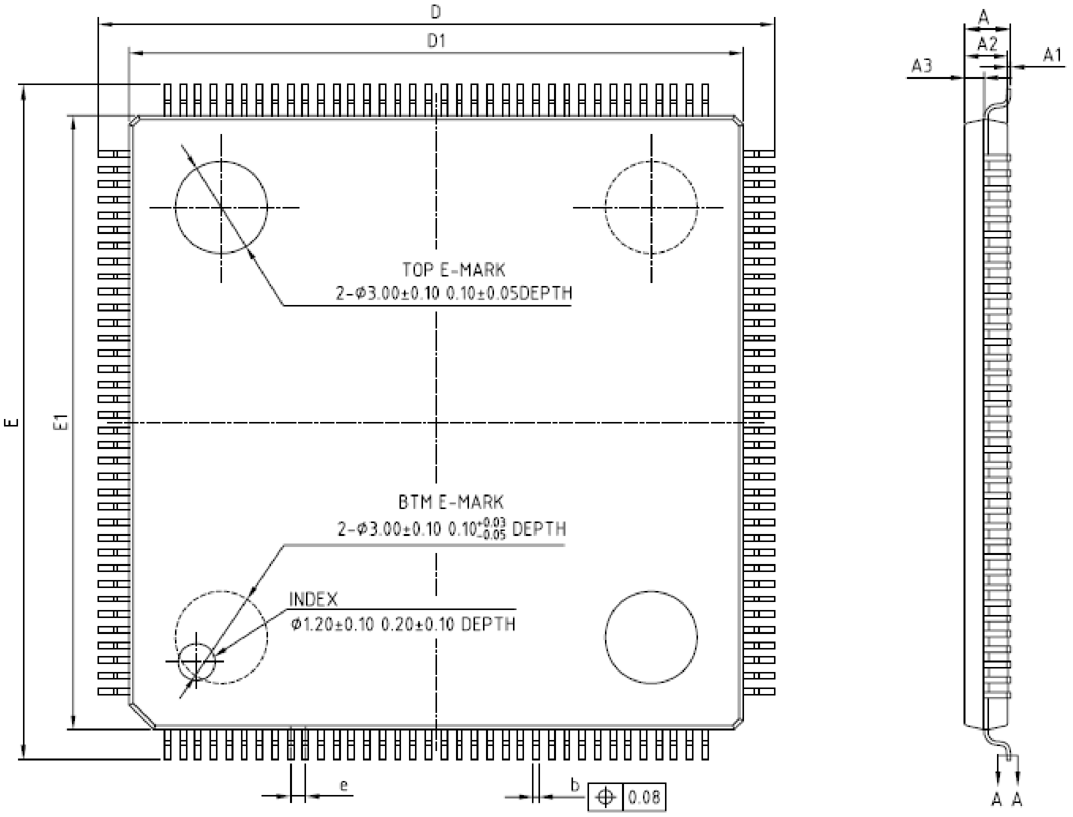
# 2. PACKAGE SIZE AND PINS

## (1) Package Dimensions

Table 1 Outline Dimensions Numerical Table

in millimeters

| DIMENSION SYMBOL | VALUE | | | DIMENSION SYMBOL | VALUE | | |
|---|---|---|---|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM | | MINIMUM | TYPICAL | MAXIMUM |
| **D** | 21.80 | 22.00 | 22.20 | **A** | n/a | n/a | 1.60 |
| **D1** | 19.90 | 20.00 | 20.10 | **A1** | 0.05 | n/a | 0.15 |
| **E.** | 21.80 | 22.00 | 22.20 | **A2** | 1.35 | 1.40 | 1.45 |
| **E1** | 19.90 | 20.00 | 20.10 | **A3** | 0.59 | 0.64 | 0.69 |
| **e** | 0.40 | 0.50 | 0.60 | **b** | 0.17 | n/a | 0.27 |
| **L** | 0.45 | 0.60 | 0.75 | **b1** | 0.17 | 0.20 | 0.23 |
| **c** | 0.127 | n/a | 0.18 | **c1** | 0.119 | 0.127 | 0.135 |



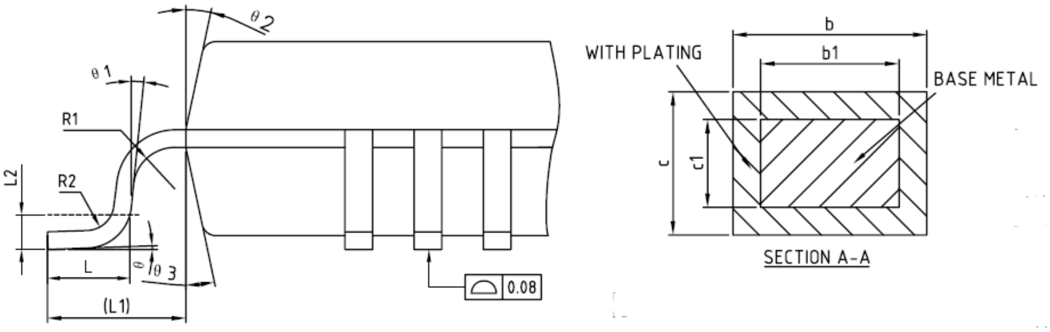



Figure 1 Outline Dimensions (POD )

## (2) Pin description

Table 2 Product pin definition

| PIN NAME | PIN TYPE | PIN DESCRIPTION |
|---|---|---|
| **USER IO PIN** | | |
| DIFFIO_[L0,L1, L2,R0,R1, R2] _ [0…n] _ [N, P] | INPUT/ OUTPUT | All common USER IOs are marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0„n]_[N,P]. DIFFIO: Indicates that all user IOs support differential input and output, such as LVDS; [L0 , L1, L2, R0, R1, R2]: indicates the bank name [0„n]: indicates the unique differential pair number in the bank; [N, P]: N indicates the negative terminal of the differential pair, P indicates the positive terminal of the differential pair end. |
| **REUSE PIN** | | |
| DIFFIO_[L0,L1,L2,R0,R1,R2 ]_[0…n]_[N,P]/XXX | | The multiplexed PIN is marked as DIFFIO_[L0,L1,L2,R0,R1,R2]_[0„n]_[N,P]/XXX, where XXX represents one or several functions described below. When the multiplexed PIN is not used for special applications, it can be used as a normal USER IO |
| **-- CONFIGURE PIN** | | |
| MODE_2, MODE_1, MODE_0 | INPUT | When configuring, it is used for configuration mode selection, as follows:<br>000: JTAG<br>001 : Master SPI ( X1 , X2 , X4 , X8 )<br>010 : master BPI ( X8 , X16 )<br>011 : Slave String ( X1 )<br>100 : Slave and ( X8 , X16 , X32 )<br>101 : From SPI ( X1 )<br>111 : internal main SPI ( X1 , X2 , X4 ) |
| INIT_FLAG_N | BIDIRECTIONAL (OPEN-DRAIN) | During configuration, when the FPGA is powered on, drive this PIN to a low level. When the FPGA initialization is complete, release the driver for this PIN. During configuration, this PIN is output as an indication of configuration errors. At the same time, during the configuration or initialization process, the PIN can be externally input with a low level to indicate an error or delayed configuration. |
| CFG_CLK | INPUT/ OUTPUT | Configure the clock PIN. In slave mode, this PIN is used as a clock input to obtain configuration data from the outside; in master mode, this PIN is used as a clock output to obtain configuration data from the outside. |
| D[31 , 30 … 1 , 0] | INPUT/ OUTPUT | 32-bit configuration data bus input and output pins:<br>(1) In the main SPI X1 configuration mode, pin D[0] is connected to the data input terminal of SPI flash as a command output, and pin D[1] is |

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|---|---|---|
| | | connected to SPI as a data input The data output terminal of flash.<br>(2) In master SPI X2 configuration mode, pin D[1:0] is the data bus.<br>(3) In master SPI X4 configuration mode, pin D[3:0] is the data bus.<br>(4) In the master SPI X8 configuration mode, pin D[3:0] is the data bus of the first SPI FLASH, and pin D[7:4] is the data bus of the second SPI FLASH.<br>(5) In the slave serial configuration mode, the pin D[1] is the data bus.<br>(6) In slave SPI configuration mode, pin D[0] is master device output, slave device input, pin D[1] master device input slave device output, pin D[3] is chip hold.<br>(7) When the main BPI configures the X8 asynchronous mode, the pin D[7:0] is an 8-bit data bus.<br>(8) When the main BPI configures X16 asynchronous/synchronous mode, pin D[15:0] is a 16-bit data bus.<br>(9) In slave parallel X8 configuration mode, pin D[7:0] is an 8-bit data bus.<br>(10) In parallel X16 configuration mode, pin D[15:0] is a 16-bit data bus.<br>(11) In parallel X32 configuration mode, pin D[31:0] is a 32-bit data bus. |
| CS_N | INPUT | Reuse configuration PIN. Chip select input, active low.<br>(1) Enable slave parallel mode configuration interface for low level.<br>(2) In other configuration modes, this PIN is in a high-impedance state.<br>(3) If you want to continue to use it as a configuration function after the configuration is completed, you need to set the configuration register and choose to keep it as a configuration function. |
| RWSEL | INPUT | Reuse configuration PIN. Read and write select input from parallel configuration mode, high for read, low for write. (1) High level, read data from the data bus in parallel configuration mode;<br>(2) Low level, write data to the data bus from the parallel configuration mode;<br>(3) The switching between reading and writing can only be switched when CS_N is high.<br>(4) If you want to continue to use it as a configuration function after the configuration is completed, you need to set the configuration register and choose to keep it as a configuration function.<br>(5) In other configuration modes, this PIN is in a high-impedance state. |

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| BUSY | OUTPUT | Reuse configuration PIN.<br>(1) During readback using parallel slave mode, the output is high to indicate that the data read from the bus is invalid data.<br>(2) If you want to continue to use it as a configuration function after entering user mode, you need to set the configuration register and choose to keep it as a configuration function.<br>(3) In other configuration modes, this PIN is in a high-impedance state. |
| CSO_DOUT | OUTPUT | Reuse configuration PIN. It needs to be used when cascading.<br>(1) Master SPI, X1 mode, as cascade data output;<br>(2) Slave serial mode configuration, output as cascade data;<br>(3) Slave parallel mode configuration, output as chip select signal; |
| FCS_N | OUTPUT | Multiplexing configuration PIN, used in external master SPI configuration mode.<br>(1) In the main SPI mode, the active low output chip select signal is sent to the external flash; |
| VS1, VS0 | INPUT | Multiplexing configuration PIN, used in master SPI or internal master SPI mode.<br>(1) data stream version selection,<br>00, select the first data stream,<br>01, select the second data stream,<br>10. Select the third data stream,<br>11. Select the fourth data stream;<br>(2) During configuration, enable the built-in pull-down resistor. |
| IO_STATUS_C | INPUT | Multiplex PIN, input signal, control the status of all user IOs during the configuration process.<br>(1) "1", make all user IOs in the pull-up state during the configuration process.<br>(2) "0", make all user IOs in tri-state during the configuration process. |
| ADR[25:0] | OUTPUT | Multiplexing configuration PIN, used in BPI configuration mode, address output in BPI configuration mode |
| BFOE_N | OUTPUT | Multiplex configuration PIN, used in BPI configuration mode; provide low level output enable control signal for parallel NOR FLASH<br>(1) In BPI configuration mode, the PAD needs to be connected to the output enable input of the flash and also needs to connect a 4.7K resistor to VCCIO. |
| BADRVO_N | OUTPUT | Multiplex configuration PIN, used in BPI configuration mode; provide low-level address valid control signal for parallel NOR FLASH;<br>(1) In BPI configuration mode, if the external FLASH supports address valid signal input, then the PAD needs to be connected to the address valid input pin of the flash and also needs to connect a 4.7K resistor to VCCIO. If the external flash does not support valid address signal input, |

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| | | then the PAD does not need to be connected. |
| BFWE_N | OUTPUT | Multiplex configuration PIN, used in BPI configuration mode; provide low-level write enable signal for parallel NOR FLASH.<br>(1) BPI configuration mode, the PAD needs to be connected to the write enable input of the flash and needs to connect a 4.7K resistor to VCCIO; |
| BFCE_N | OUTPUT | Multiplexing configuration PIN, used in BPI configuration mode; provide low-level chip selection control signal for parallel NOR FLASH;<br>(1) In BPI configuration mode, D needs to be connected to the chip select input of the flash and also needs to connect a 4.7K resistor to VCCIO. |
| FCS2_N | OUTPUT | Multiplexing configuration PIN, used in external master SPI X8 configuration mode.<br>(1) In the main SPI X8 mode, the active-low output chip select signal is sent to the external flash; an external pull-up resistor is required not greater than 4.7K to VCCIO |
| ECCLKIN | INPUT | Multiplexing configuration PIN, input signal, clock input for internal master configuration mode |
| **--Clock , PLL , crystal multiplexing PIN** | | |
| CLK[0,1,2,3]_[L0, L1,L2, R0,R1,R2] | INPUT | Dedicated global clock input PIN, each bank provides 4 PINs |
| DIFFCLK[0,1]_[L0 ,L1,L2,R0,R1,R2] _[N,P] | INPUT | Dedicated global differential clock input PIN, each bank provides 2 pairs |
| PLL[0,1,2,… 10]_CLKOUT_[P, N] | OUTPUT | Can directly select the output of PLL [0 , 1,…,19] to PAD |
| PLL[0,1,2,… 10]_CLKIN [0,1,2,3] | INPUT | Optional PLL input, PLL can choose to input clock directly from these pads |
| PLL[0,1,2,…10 ] _CLKFB_[P,N] | INPUT | Optional PLL feedback clock input, PLL can choose external feedback clock from these pads |
| XTALA_[L0,L1,L2, R0,R1,R2] | INPUT | Dedicated external crystal A terminal input. It is the input of the on-chip inverter, each bank provides 1 PIN |
| XTALB_[L0,L1,L2, R0,R1,R2] | OUTPUT | Dedicated external crystal B terminal output. It is the output of the on-chip inverter, each bank provides 1 PIN |
| **--External memory interface PIN** | | |
| DQS[0,1,2] [#]_[L0,L1,L2, R0,R1,R2] | Input/ Output OUT | DQS/DQS# signal pin connection for external memory |
| DQ[0,1,2]_[L0,L1 ,L2, R0,R1, R2] | Input/ Output OUT | DQ signal pin connection available for external memory |
| **--HMEMC Memory interface PIN** | | |
| [R,L]_A[0,…,15] | OUTPUT | DDR memory address |
| [R,L]_CS_N | OUTPUT | Chip select signal of DDR memory, low effective, depends on whether the memory is used. |
| [R,L]_RAS_N | OUTPUT | RAS , active low |

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|---|---|---|
| [R,L]_CAS_N | OUTPUT | CAS , active low |
| [R,L]_WE_N | OUTPUT | Write enable, active low |
| [R,L]_BA[0,1,2] | OUTPUT | ddr sdram BANK address |
| [R,L]_ODT | OUTPUT | ODT , On-Die Termination |
| [R,L]_CK | OUTPUT | ddr memory clock P |
| [R,L]_CK_N | OUTPUT | ddr memory clock N |
| [R,L]_CKE | OUTPUT | ddr Memory clock enable, active high |
| [R,L]_RESET_N | OUTPUT | ddr Memory reset, active low |
| [R,L]_DML | OUTPUT | DQ0-DQ7 write data mask signal |
| [R,L]_DQSL | INPUT/ OUTPUT OUT | DQ0-DQ7 Related DQS signal |
| [R,L]_DQSL_N | INPUT/ OUTPUT OUT | DQ0-DQ7 Associated DQS# signal |
| [ R, L]_DQ [0, …,15] | INPUT/ OUTPUT OUT | memory data bus |
| [R,L]_DMU | OUTPUT | DQ8-DQ15 The write data mask signal |
| [R,L]_DQSU | INPUT/ OUTPUT OUT | DQ8-DQ15 related DQS signal |
| [R,L]_DQSU_N | INPUT/ OUTPUT OUT | DQ8-DQ15 related DQS# signal |
| [R,L]_DQSL_GATE_IN | INPUT | Compensates for the DQS gate window signal (low) that comes back after the read command path delay |
| [R,L]_DQSL_GATE_OUT | OUTPUT | DQS gate window signal (low) output after compensating for read command path delay |
| [R,L]_DQSU_GATE_IN | INPUT | Compensates for the DQS gate window signal (high) that comes back after the read command path delay |
| [R,L]_DQSU_GATE_OUT | OUTPUT | DQS gate window signal (high) output after compensating for read command path delay |
| **--REFERENCE PIN** | | |
| RRP_[L0,L1,L2,R0, R1,R2] | INPUT | External reference resistors PIN, one per bank. Used for on-chip termination resistor adjustment to provide a reference resistance to the power supply. |
| RRN_[L0,L1,L2,R0, R1,R2] | INPUT | External reference resistors PIN, one per bank. Used for on-chip termination resistor adjustment to provide a reference resistor to ground. |
| VREF_[L0,L1,L2,R 0,R1,R2] | INPUT | External reference power supply PINs, one for each bank Used to provide reference voltage input for each BANK |
| **--ADC PIN** | | |
| VAUX[9,8,7,..0] | INPUT | Input analog signal |
| **DEDICATED PIN** | | |
| **--CONFIGURATION , JTAG PIN** | | |

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| CFG_DONE | BIDIRECTIONAL AL (OPEN-DRAIN) | A dedicated PIN for configuration status is used as a status output, which is driven low before or during configuration. Once all configuration data has been properly received and start-up timing has been initiated, control of this PIN is released. |
| RST_N | INPUT | Dedicated configuration input PIN, internal weak pull-up, is used to restart the configuration process, low active. It is recommended that users pull up RST_N with a resistor outside the chip during use. when this PIN is low, the FPGA enters reset state and all IOs are in HighZ state. |
| TCK | INPUT | Dedicated JTAG Test Clock Clock Input PIN |
| TMS | INPUT | Dedicated JTAG Test mode selection input PIN |
| TDI | INPUT | Dedicated JTAG test data entry PIN . |
| TDO | OUTPUT | Dedicated JTAG Test data output PIN . |
| **--REFERENCE PIN _** | | |
| REXT | INPUT | Dedicated external high precision resistor pin with 10k resistance value and 1% accuracy. Provide resistance to bandgap. |
| **--ADC PIN** | | |
| VA[1,0] | INPUT | Dedicated analog input signal |
| VREF_EXT | INPUT | Dedicated external reference 2.5V voltage. |
| **POWER, GROUND PIN** | | |
| VCC | POWER | Core power supply, 1.1V. Provides power to the core logic |
| VCCAUX | POWER | Auxiliary 3.3V power supply to provide auxiliary power to IOB, LDO and other modules |
| VDDIO[L0,L1,L2, R0,R1, R2] | POWER | IO BANK power supply, the left bank from top to bottom is BANKL0, BANKL1, BANKL2, and so on; the right BANK, from top to bottom is BANKR0, BANKR1, BANKR2, and so on |
| VCCAUX_A | POWER | ADC , BANDGAP , POR power supply |
| VSS | GR0UND | GND relative to VCC&VCCAUX |
| VSSA | GR0UND | GND relative to VCCAUX_A |
| VDDEFUSE | POWER | EFUSE programming voltage |
| VDDIOCFG | POWER | BANKCFG power supply |

Remark : PGL12G_LPG144 product user IO The number is 103 .

# 3. PIN NAME LIST

Table 3 Pin name list

| PIN NUMBER | PIN(FUNCTION) NAME |
|---|---|
| 1 | DIFFIO_R0_7_N/VS0 |
| 2 | DIFFIO_R0_7_P/VS1 |
| 3 | DIFFIO_R0_4_P/FCS2_N |
| 4 | DIFFIO_R0_3_N/ECCLKIN |
| 5 | DIFFIO_R0_2_P/VAUX1 |
| 6 | VCCAUX |
| 7 | DIFFIO_R0_1_N/VAUX2 |
| 8 | DIFFIO_R0_1_P/VAUX3 |
| 9 | VDDIOR0 |
| 10 | DIFFIO_R0_0_P/VAUX5 |
| 11 | DIFFIO_R0_0_N/VAUX4 |
| 12 | VSS |
| 13 | VCC |
| 14 | VCCAUX_A |
| 15 | VDDEFUSE |
| 16 | TCK |
| 17 | TDO |
| 18 | TMS |
| 19 | TDI |
| 20 | VDDIOCFG |
| 21 | RST_N |
| 22 | CFG_DONE |
| 23 | REXT |
| 24 | VCCAUX_A |
| 25 | VSS |
| 26 | VCC |
| 27 | VSS |
| 28 | DIFFIO_L0_0_P/BUSY |
| 29 | VDDIOL0 |
| 30 | DIFFIO_L0_3_P/IO_STATUS_C |
| 31 | DIFFIO_L0_3_N/CFG_CLK |
| 32 | DIFFIO_L0_5_P/MODE_0 |
| 33 | DIFFIO_L0_5_N/MODE_1 |
| 34 | DIFFIO_L0_4_P/FCS_N |
| 35 | DIFFIO_L0_4_N/CS_N |
| 36 | DIFFIO_L0_7_P/RWSEL |
| 37 | DIFFIO_L0_6_P/MODE_2 |
| 38 | DIFFIO_L0_7_N/INIT_FLAG_N |

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|---|---|
| 39 | DIFFIO_L0_6_N/VREF_L0/CSO_DOUT |
| 40 | DIFFIO_L0_8_P/PLL0_CLKOUT_P |
| 41 | DIFFIO_L0_8_N/PLL0_CLKOUT_N |
| 42 | DIFFIO_L0_9_P/CLK0_L0/DIFFCLK0_L0_P/ PLL0_CLKFB_P/XTALA_L0 |
| 43 | DIFFIO_L0_9_N/CLK1_L0/DIFFCLK0_L0_N/ PLL0_CLKFB_N/XTALB_L0 |
| 44 | DIFFIO_L0_10_P/CLK2_L0/DIFFCLK1_L0_P/PLL1_CLKIN0 |
| 45 | DIFFIO_L0_10_N/CLK3_L0/DIFFCLK1_L0_N/PLL1_CLKIN1 |
| 46 | DIFFIO_L0_11_P/PLL1_CLKIN2 |
| 47 | DIFFIO_L0_11_N/PLL1_CLKIN3 |
| 48 | DIFFIO_L0_12_P/D0 |
| 49 | DIFFIO_L0_12_N/RRN_L0/D1 |
| 50 | DIFFIO_L0_13_P/RRP_L0/D2 |
| 51 | DIFFIO_L0_13_N/D3 |
| 52 | DIFFIO_L0_14_P/D4 |
| 53 | DIFFIO_L0_14_N/D5 |
| 54 | DIFFIO_L0_15_P/D6 |
| 55 | DIFFIO_L0_15_N/D7 |
| 56 | VDDIOL0 |
| 57 | VSS |
| 58 | DIFFIO_L1_2_P |
| 59 | DIFFIO_L1_2_N |
| 60 | DIFFIO_L1_4_P |
| 61 | DIFFIO_L1_4_N |
| 62 | VDDIOL1 |
| 63 | VCCAUX |
| 64 | DIFFIO_L1_6_N/VREF_L1 |
| 65 | DIFFIO_L1_8_P/PLL2_CLKOUT_P |
| 66 | DIFFIO_L1_8_N/PLL2_CLKOUT_N |
| 67 | VCC |
| 68 | VSS |
| 69 | DIFFIO_L1_11_P/PLL3_CLKIN2 |
| 70 | DIFFIO_L1_10_N/CLK3_L1/DIFFCLK1_L1_N/PLL3_CLKIN1 |
| 71 | DIFFIO_L1_11_N/PLL3_CLKIN3 |
| 72 | DIFFIO_L1_13_P/RRP_L1 |
| 73 | DIFFIO_L1_12_N/RRN_L1 |
| 74 | DIFFIO_L1_15_P |
| 75 | DIFFIO_L1_15_N |
| 76 | DIFFIO_L1_17_P |
| 77 | DIFFIO_L1_17_N |
| 78 | VSS |
| 79 | DIFFIO_L1_16_N |
| 80 | DIFFIO_L1_18_P |
| 81 | DIFFIO_L1_18_N |
| 82 | VSS |

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|---|---|
| 83 | VDDIOL1 |
| 84 | DIFFIO_L1_19_N |
| 85 | DIFFIO_L1_19_P |
| 86 | DIFFIO_L1_10_P/CLK2_L1/DIFFCLK1_L1_P/PLL3_CLKIN0 |
| 87 | DIFFIO_L1_9_N/CLK1_L1/DIFFCLK0_L1_N/ PLL2_CLKFB_N/XTALB_L1 |
| 88 | DIFFIO_L1_9_P/CLK0_L1/DIFFCLK0_L1_P/ PLL2_CLKFB_P/XTALA_L1 |
| 89 | VCC |
| 90 | VSS |
| 91 | VCCAUX |
| 92 | DIFFIO_R1_9_P/CLK0_R1/DIFFCLK0_R1_P/ PLL2_CLKIN2/XTALA_R1 |
| 93 | DIFFIO_R1_9_N/CLK1_R1/DIFFCLK0_R1_N/ PLL2_CLKIN3/XTALB_R1 |
| 94 | DIFFIO_R1_10_P/CLK2_R1/DIFFCLK1_R1_P/ PLL3_CLKFB_P |
| 95 | DIFFIO_R1_19_P |
| 96 | DIFFIO_R1_19_N |
| 97 | DIFFIO_R1_10_N/CLK3_R1/DIFFCLK1_R1_N/ PLL3_CLKFB_N |
| 98 | VDDIOR1 |
| 99 | DIFFIO_R1_18_N |
| 100 | DIFFIO_R1_18_P |
| 101 | DIFFIO_R1_16_N |
| 102 | DIFFIO_R1_16_P |
| 103 | DIFFIO_R1_14_N |
| 104 | VSS |
| 105 | DIFFIO_R1_17_N |
| 106 | DIFFIO_R1_17_P |
| 107 | DIFFIO_R1_15_N |
| 108 | DIFFIO_R1_15_P |
| 109 | DIFFIO_R1_12_N/RRN_R1 |
| 110 | DIFFIO_R1_13_P/RRP_R1 |
| 111 | DIFFIO_R1_11_N/PLL3_CLKOUT_N |
| 112 | DIFFIO_R1_11_P/PLL3_CLKOUT_P |
| 113 | VDDIOR1 |
| 114 | VSS |
| 115 | VCC |
| 116 | DIFFIO_R1_8_N/PLL2_CLKIN1 |
| 117 | DIFFIO_R1_8_P/PLL2_CLKIN0 |
| 118 | DIFFIO_R1_6_N/VREF_R1 |
| 119 | VDDIOR1 |
| 120 | DIFFIO_R1_4_N/ADR24 |
| 121 | DIFFIO_R1_4_P/ADR23 |
| 122 | DIFFIO_R1_2_N/ADR20 |
| 123 | DIFFIO_R1_2_P/ADR19 |

| | |
|---|---|
| 124 | VCCAUX |
| 125 | VSS |
| 126 | VDDIOR0 |
| 127 | DIFFIO_R0_15_N/D23/ADR7 |
| 128 | DIFFIO_R0_15_P/D22/ADR6 |
| 129 | DIFFIO_R0_14_N/D21/ADR5 |
| 130 | DIFFIO_R0_14_P/D20/ADR4 |
| 131 | DIFFIO_R0_13_N/D19/ADR3 |
| 132 | DIFFIO_R0_13_P/RRP_R0/D18/ADR2 |
| 133 | DIFFIO_R0_12_N/RRN_R0/D17/ADR1 |
| 134 | DIFFIO_R0_11_N/PLL1_CLKOUT_N |
| 135 | DIFFIO_R0_12_P/D16/ADR0 |
| 136 | DIFFIO_R0_11_P/PLL1_CLKOUT_P |
| 137 | DIFFIO_R0_10_N/CLK3_R0/DIFFCLK1_R0_N/ PLL1_CLKFB_N |
| 138 | DIFFIO_R0_10_P/CLK2_R0/DIFFCLK1_R0_P/ PLL1_CLKFB_P |
| 139 | DIFFIO_R0_9_N/CLK1_R0/DIFFCLK0_R0_N/ PLL0_CLKIN3/XTALB_R0 |
| 140 | VDDIOR0 |
| 141 | DIFFIO_R0_9_P/CLK0_R0/DIFFCLK0_R0_P/ PLL0_CLKIN2/XTALA_R0 |
| 142 | DIFFIO_R0_8_N/PLL0_CLKIN1 |
| 143 | DIFFIO_R0_8_P/PLL0_CLKIN0 |
| 144 | DIFFIO_R0_6_N/VREF_R0 |